

Sub AI

Figure 1 consists of 15 bar charts arranged in a grid. The first 10 charts show protein types A through J, and the last 5 charts show protein types K through O. Each chart has a y-axis labeled 'Percentage of total protein' and an x-axis labeled 'Fraction'. The fractions are labeled A, B, C, D, E, F, G, H, I, J, K, L, M, N, O. The data is presented in a table below.

Protein Type	Fraction	Percentage of total protein
A	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
B	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
C	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
D	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
E	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
F	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
G	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
H	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
I	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
J	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
K	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
L	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
M	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
N	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100
O	A	100
	B	100
	C	100
	D	100
	E	100
	F	100
	G	100
	H	100
	I	100
	J	100

method of operation comprising:
register with a counter;
be executed;
executing a loop;
repeatedly executing
at least one action;
at least one action;
.

method of operation comprising:
g:
REPEAT instruction;
REPEAT instruction;
er a count variable;
be executed;
one or more actions;
associated instruction;

method of operation comprising:
g:
register with a counter;
ns are to be executed;

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fetching and executing a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

incrementing a program counter;

fetching the one or more associated instructions; and

executing the one or more associated instruction for as many times as indicated by a count value stored in a count register.

4. A method of operating a processor according to claim 3, wherein said count value is stored in said count register before execution of said REPEAT instruction.

5. A method of operating a processor according to claim 3, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

6. A method of operating a processor according to claim 3, wherein said method further comprises:

incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

7. A method according to claim 3, wherein method further comprises: decrementing said count value stored in said register each time said one or more associated instructions are executed; and

determining whether said count value is less than or equal to zero.

Figure 1 consists of 12 bar charts, each representing a different demographic or marital category. The x-axis for all charts represents age groups: 18-24, 25-34, 35-44, 45-54, 55-64, 65-74, and 75+. The y-axis represents the percentage of the total sample, ranging from 0 to 100. The categories are: 1. Total sample, 2. Male, 3. Female, 4. White, 5. Black, 6. Hispanic, 7. Asian, 8. Pacific Islander, 9. Other, 10. Married, 11. Single, and 12. Divorced. The charts show that the distribution of these categories varies significantly with age. For example, the 'Married' category (10) shows a high percentage in the 45-54 age group, while the 'Single' category (11) is highest in the 18-24 age group. The 'Divorced' category (12) is most prevalent in the 55-64 age group.

8. A processor for repeatedly execute at least one associated

load means for loading a register with a count value indicative of the

first fetch means for a REPEAT instruction indicating the at least one

first execute means for ~~executing~~ the REPEAT instruction indicating the at

second fetch means for fetching the at least one associated instruction; and

first execute means for executing the at least one associated instruction for

9. A processor for repeatedly executing one or more instructions,

first fetch means for fetching a REPEAT instruction;

first execute means for executing a REPEAT instruction, wherein

second fetch means for fetching the one or more associated instructions;

and

second execute means for executing the associated instruction for as many

10. A processor for repeatedly executing one or more instructions,

load means for loading a register with a count value indicative of the

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first fetch means for fetching a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

means for incrementing a program counter;

second fetch means for fetching the one or more associated instructions;

and

second execute means for executing the one or more associated instruction for as many times as indicated by a count value stored in a count register.

11. A processor according to claim 10, wherein said count value is stored in said count register before execution of said REPEAT instruction.

12. A processor according to claim 10, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

13. A processor according to claim 10, wherein said processor further comprises:

means for incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

14. A processor according to claim 10, wherein processor further comprises:

means for decrementing said count value stored in said register each time said one or more associated instructions are executed; and

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means for determining whether said count value is less than or equal to zero.

15. A processor for repeatedly executing one or more processor instructions, said processor comprising

- a memory address register associated with a main memory;
- a memory data register associated with the main memory;
- a memory control for generating memory control signals;
- a program counter for storing a memory address location of the main memory where an instruction is to be fetched;
- an instruction register for storing an instruction that is to be executed;
- at least one general purpose register;
- decode and execute control logic for decoding and executing an instruction stored in the instruction register; and
- a state machine for controlling the fetching and repeated execution of one or more associated instructions.

16. A processor according to claim 15, wherein said processor further comprises an instruction buffer for storing the one or more associated instructions.

17. A processor according to claim 15, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed.

18. A processor according to claim 17, wherein said state machine generates signals for decrementing the count value stored in the first register.

